WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device, comprising:

a plurality of floating gate field effect transistors each having a control gate, a floating gate, a drain and a source and capable of electrically writing and erasing data, the floating gate field effect transistors being arrayed in a matrix on a substrate or a well;

a plurality of row lines each connected to control gates of the floating gate field effect transistors arrayed in a row direction;

a plurality of column lines each connected to drains of the floating gate field effect transistors arrayed in a column direction;

a common source line connected to sources of the floating gate field effect transistors constituting a block;

a regulator circuit for supplying a voltage applied to the common source line at least during erasure;

a resistance element inserted between the regulator circuit and an external power source;

voltage level detecting means for instructing start of the erase voltage application to the common source line, detecting that an input voltage from the resistance element to the regulator circuit reaches a prescribed

voltage level and instructing termination of the erase voltage application to the common source line; and

erase voltage applying means for receiving an instruction from the voltage level detecting means and applying an erase voltage from the regulator circuit to the common source line.

2. The nonvolatile semiconductor memory device according to Claim 1, further comprising:

a voltage boosting circuit provided between the external power source and the resistance element, wherein

an output voltage from the voltage boosting circuit is supplied to the regulator circuit via the resistance element.

3. The nonvolatile semiconductor memory device according to Claim 1, wherein

the prescribed voltage level detected by the voltage level detecting means is a voltage higher than the erase voltage applied to the common source line.

4. The nonvolatile semiconductor memory device according to Claim 2, wherein

the prescribed voltage level detected by the voltage level detecting means is a voltage higher than the erase voltage applied to the common source line.

5. The nonvolatile semiconductor memory device according to Claim 1, wherein

a resistance value of the resistance element is set at {a voltage of the external power source - the erase voltage}/{a maximum value of erase current}.

6. The nonvolatile semiconductor memory device according to Claim 2, wherein

a resistance value of the resistance element is set at {the output voltage of the voltage boosting circuit during erasure - the erase voltage}/{a maximum value of erase current}.

7. The nonvolatile semiconductor memory device according to Claim 1, wherein

an output voltage of the external power source during erasure is a voltage higher than the erase voltage.

8. The nonvolatile semiconductor memory device according to Claim 2, wherein

an output voltage of the voltage boosting circuit during erasure is a voltage higher than the erase voltage.

9. The nonvolatile semiconductor memory device according to Claim 7, wherein

the voltage of the external power source during erasure is 9 V or higher.

10. The nonvolatile semiconductor memory device according to Claim 8, wherein

the output voltage of the voltage boosting circuit during erasure is 9 V or higher.

11. A method of erasing a nonvolatile semiconductor memory device in which floating gate field effect transistors each having a control gate, floating gate, drain and source and capable of electrically writing and erasing data are arrayed in a matrix on a substrate or a well, a plurality of row lines connected to control gates floating gate field effect transistors arrayed in a row direction and a plurality of column lines connected to drains of floating gate field effect transistors arrayed in a column direction are included and sources of the floating gate field effect transistors constituting a block are connected to a common source line, the method comprising:

a first erase operation for continuing to apply an erase voltage to the common source line; and

a second erase operation for repeating erase pulse application to the common source line and an erase-verify operation alternately,

wherein a current value flowing between a stabilization circuit for generating a voltage applied to the common source line and a power source of this stabilization circuit is detected during the first operation and when the current value reaches a prescribed current value, the first erase operation is stopped and the second erase operation is started.

12. The method of erasing a nonvolatile semiconductor

memory device according to Claim 11, wherein

the power source of the stabilization circuit is an internal voltage boosting circuit.